AMENDMENTS TO THE CLAIMS

This listing of claims replaces all previous versions and listings of claims in this application.

Claim Listing:

1. (Currently amended) A method for decoding multiword information, comprising the steps of:

providing a multiword information cluster including high protective codewords and low protective codewords;

storing the low protective codewords into a first memory;

decoding the high protective codewords so as to generate high protective word erasure indicators showing whether decoding errors occur;

storing the high protective word erasure indicators into a second memory;

decoding the low protective codewords read from the first memory by means of an erasure indicator read from the second memory; and

marking an erasure ~~indicator~~ bit for decoding the low protective codewords based on the high protective word erasure indicators close to any low protective codeword in the multiword information cluster,

wherein the erasure bit is determined by automatically switching strategies to be more strict in sequence.

2. (Original) The method for decoding multiword information in accordance with Claim 1, wherein the multiword information cluster is an error correction code (ECC) cluster,

and the high and low protective codewords are burst indicator subcodes (BIS) and long-distance codes (LDC), respectively.

3. (Original) The method for decoding multiword information in accordance with Claim 1, further comprising the steps of:

detecting errors of synchronization codes included in the multiword information cluster so as to generate sync erasure indicators; and

storing the sync erasure indicators into the first memory;

wherein the sync erasure indicators function as the high protective word erasure indicators for generating the erasure bit while the low protective codewords are being decoded.

4. (Original) The method for decoding multiword information in accordance with Claim 2, wherein the BIS codes include address field information, and the high protective word erasure indicators are determined by decoding errors or address comparison faults of the address field information.

5. (Original) The method for decoding multiword information in accordance with Claim 2, wherein the BIS codes include user control data, and the high protective word erasure indicators are determined by the user control data.

6. (Original) The method for decoding multiword information in accordance with Claim 1, wherein the erasure bit is marked if at least one of the high protective word erasure indicators close to the low protective codewords shows an error.

7. (Original) The method for decoding multiword information in accordance with Claim 1, wherein the high and low protective codewords are de-interleaved before being stored into the first memory.

8. (Currently amended) The method for decoding multiword information in accordance with Claim 1, wherein the ~~erasure bit is determined by a flexible strategy, which is switched automatically from one to another strategy~~strategies comprise:

a first strategy in which the erasure bit is marked if one high protective word erasure indicator exists at a high protective codeword next to the low protective codeword at each side;

a second strategy in which the erasure bit is marked if one high protective word erasure indicator exists at one of the two high protective codewords next to the low protective codeword at each side;

a third strategy in which the erasure bit is marked if two high protective word erasure indicators exist at two high protective codewords next to the low protective codeword at one side; and

a fourth strategy in which the erasure bit is marked if only one high protective word erasure indicator exists at a high protective codeword next to the low protective codeword at one side.

9. (Original) The method for decoding multiword information in accordance with Claim 1 wherein the second memory is initialized before a new multiword information cluster is decoded.

10. (Original) The method for decoding multiword information in accordance with Claim 3, wherein the second memory is initialized with sync erasure indicators before a new multiword information cluster is decoded.

11. (Currently amended) A method for decoding multiword information, comprising the steps of:

storing low protective codewords of the multiword information into a memory;

decoding high protective codewords of the multiword information so as to generate high protective word erasure indicators showing whether decoding errors occur;

storing the high protective word erasure indicators into the memory;

decoding the low protective codewords by means of an erasure indicator read from the memory; and

marking an erasure ~~indicator~~ bit for decoding the low protective codewords based on high protective word erasure indicators close to any low protective codeword in the multiword information cluster,

wherein the erasure bit is determined by automatically switching strategies to be more strict in sequence.

12. (Original) The method for decoding multiword information in accordance with Claim 11, wherein the multiword information cluster is an error correction code (ECC) cluster, and the high and low protective codewords are burst indicator subcodes (BIS) and long-distance codes (LDC), respectively.

13. (Original) The method for decoding multiword information in accordance with Claim 11, further comprising the steps of:

detecting errors of synchronization codes included in the multiword information cluster so as to generate sync erasure indicators; and

storing the sync erasure indicators into the memory;

wherein the sync erasure indicators function as the high protective word erasure indicators for generating the erasure bit while the low protective codewords are being decoded.

14. (Original) The method for decoding multiword information in accordance with Claim 11, wherein the high and low protective codewords are de-interleaved before being stored into the memory.

15. (Currently amended) A method for decoding multiword information, comprising the steps of:

providing a multiword information cluster including synchronization codes and low protective codewords;

detecting any error flag of the synchronization codes, so as to generate sync erasure indicators;

storing the sync erasure indicators into a memory; ~~and~~

decoding the low protective codewords by means of the sync erasure indicators; and

marking an erasure bit for decoding the low protective codewords based on the sync erasure indicators close to any low protective codeword in the multiword information cluster,

wherein the erasure bit is determined by automatically switching strategies to be more strict in sequence.

16. (Currently amended) A method for decoding multiword information, comprising the steps of:

providing a multiword information cluster including address field information, user control data and low protective codewords;

detecting any error flag of the address field information or user control data, so as to generate address field information/user control data erasure indicators;

storing the address field information/user control data erasure indicators into a memory; and

decoding the low protective codewords by means of at least one of the address field information/user control data erasure indicators; and

marking an erasure bit for decoding the low protective codewords based on the address field information/user control data erasure indicators close to any low protective codeword in the multiword information cluster,

wherein the erasure bit is determined by automatically switching strategies to be more strict in sequence.

17. (Currently amended) A method for decoding multiword information, comprising the steps of:

providing a multiword information cluster including address field information, user control data and ~~low~~ high protective codewords;

detecting any error flag of the address field information or user control data, so as to generate address field information/user control data erasure indicators;

storing the address field information/user control data erasure indicators into a memory; and

decoding the high protective codewords by means of at least one of the address field information/user control data erasure indicators; and

marking an erasure bit for decoding the high protective codewords based on the address field information/user control data erasure indicators close to any high protective codeword in the multiword information cluster,

wherein the erasure bit is determined by automatically switching strategies to be more strict in sequence.

18. (Currently amended) An apparatus for decoding multiword information, comprising:

a first memory for storing high protective codewords of a multiword information cluster, the multiword information cluster further comprising low protective codewords;

a decoder for decoding the high protective codewords and correct data to first memory so as to generate high protective word erasure indicators;

a second memory coupled to the decoder for storing the high protective word erasure indicators, wherein the second memory is isolated from the first memory; and

an erasure generator coupled to the second memory for generating erasure bits for the low protective codewords, wherein the erasure generator marks an erasure bit if high protective word erasure indicators of the second memory close to any low protective codeword in the multiword information cluster show errors,

wherein the erasure bit is determined by automatically switching strategies to be more strict in sequence.

19. (Original) The apparatus for decoding multiword information in accordance with Claim 18, further comprising a mapping circuit coupled to the decoder and the second memory for providing localities for the high protective word erasure indicators.

20. (Original) The apparatus for decoding multiword information in accordance with Claim 18, wherein the decoder is further employed to decode the low protective codeword by means of the erasure bit.

21. (Original) The apparatus for decoding multiword information in accordance with Claim 18, further comprising a de-interleaving circuit connected to the first memory for de-interleaving the high or low protective codewords.

22. (Original) The apparatus for decoding multiword information in accordance with Claim 18, further comprising a synchronization error circuit connected to the first memory for detecting errors of synchronization codes in the multiword information cluster, wherein the synchronization error circuit generates sync erasure indicators, which generate erasure bits while the low protective codewords are being decoded.

23. (Original) The apparatus for decoding multiword information in accordance with Claim 18, further comprising:

an address field and user control data mapping circuit for generating address field erasure indicators caused by a decoding error or an address error of an address field information or by user control data error.

24. (Original) The apparatus for decoding multiword information in accordance with Claim 23, further comprising:

an address field decoder connected to the address field and user control data mapping circuit for decoding the address field information.

25. (Original) The apparatus for decoding multiword information in accordance with Claim 18, wherein the multiword information cluster is an error correction code (ECC) cluster, and the high and low protective codewords are burst indicator subcodes (BIS) and long-distance codes (LDC), respectively.

26. (Original) The apparatus for decoding multiword information in accordance with Claim 18, wherein the first memory is a DRAM.

27. (Original) The apparatus for decoding multiword information in accordance with Claim 18, wherein the second memory is an SRAM.

28. (Original) The apparatus for decoding multiword information in accordance with Claim 18, wherein the second memory is initialized before a new multiword information cluster is decoded.

29. (Currently amended) An apparatus for decoding multiword information, comprising:

a memory for storing high protective codewords of a multiword information cluster, the multiword information cluster further comprising low protective codewords; and

a decoder for decoding the high protective codewords so as to generate high protective word erasure indicators with localities to the memory;

wherein an erasure bit of a low protective codeword is marked if a high protective word erasure indicator of a high protective codeword close to the low protective codeword shows errors, and the erasure bit is determined by automatically switching strategies to be more strict in sequence.

30. (Original) The apparatus for decoding multiword information in accordance with Claim 29, wherein the multiword information cluster is an error correction code (ECC) cluster, and the high and low protective codewords are burst indicator subcodes (BIS) and long-distance codes (LDC), respectively.

31. (Original) The apparatus for decoding multiword information in accordance with Claim 29, wherein the memory is a DRAM.